
# LPC1766-STK development board

## Users Manual

Pb-free, Green All boards produced by Olimex are ROHS compliant

**Revision Initial, October 2009**

## INTRODUCTION:

LPC1766-STK is development board with LPC1766 Cortex M3 microcontroller from NXP. This powerful microcontroller supports various serial interfaces such as USB Device/Host/OTG, UART, CAN and other. On the board are avalable audio input and output, digital accelerometer, JTAG, Ethernet, TFT LCD and mini SD/MMC card connector. All this allows you to build a diversity of powerful applications to be used in a wide range of applications.

## BOARD FEATURES:

- MCU: **LPC1766** Cortex M3, 100 Mhz, 256KB Flash, 64KB RAM, Ethernet MAC, USB Host/ Device/OTG, x4 UARTS, CAN, SPI, SSP, I2C, I2S, ADC, DAC, TC
- LCD NOKIA 6610 128x128 x12bit color TFT with Epson LCD controller
- 3-axis digital accelerometer with 11 bit accuracy
- temperature sensor
- Ethernet 100Mbit
- CAN interface and connector
- USB host connector
- USB device connector
- USB OTG connector
- two user LEDs
- three user buttons
- joystick
- potentiometer
- micro SD/MMC card connector
- JTAG and TRACE connectors
- power supply
- RESET circuit
- UEXT connector
- Audio IN
- Audio OUT
- RTC battery
- FR-4, 1.5 mm, red soldermask, component print
- Dimensions:134.6x101.6mm (5.3 x 4.0")

## ELECTROSTATIC WARNING:

The **LPC1766-STK** board is shipped in protective anti-static packaging. The board must not be subject to high electrostatic potentials. General practice for working with static sensitive devices should be applied when working with this board.

## BOARD USE REQUIREMENTS:

**Cables:** The cable you will need depends on the programmer/debugger you use. If you use ARM-JTAG-EW, you will need USB A-B cable. If you use a software programmer such as FlashMagic, you will need RS232 cable.

**Hardware:** Programmer/Debugger ARM-JTAG-EW or other compatible programming/debugging tool if you work with EW-ARM.

You can use also ARM-USB-OCD, ARM-USB-TINY, ARM-USB-TINY-H with CrossWorks.or OpenOCD.

## PROCESSOR FEATURES:

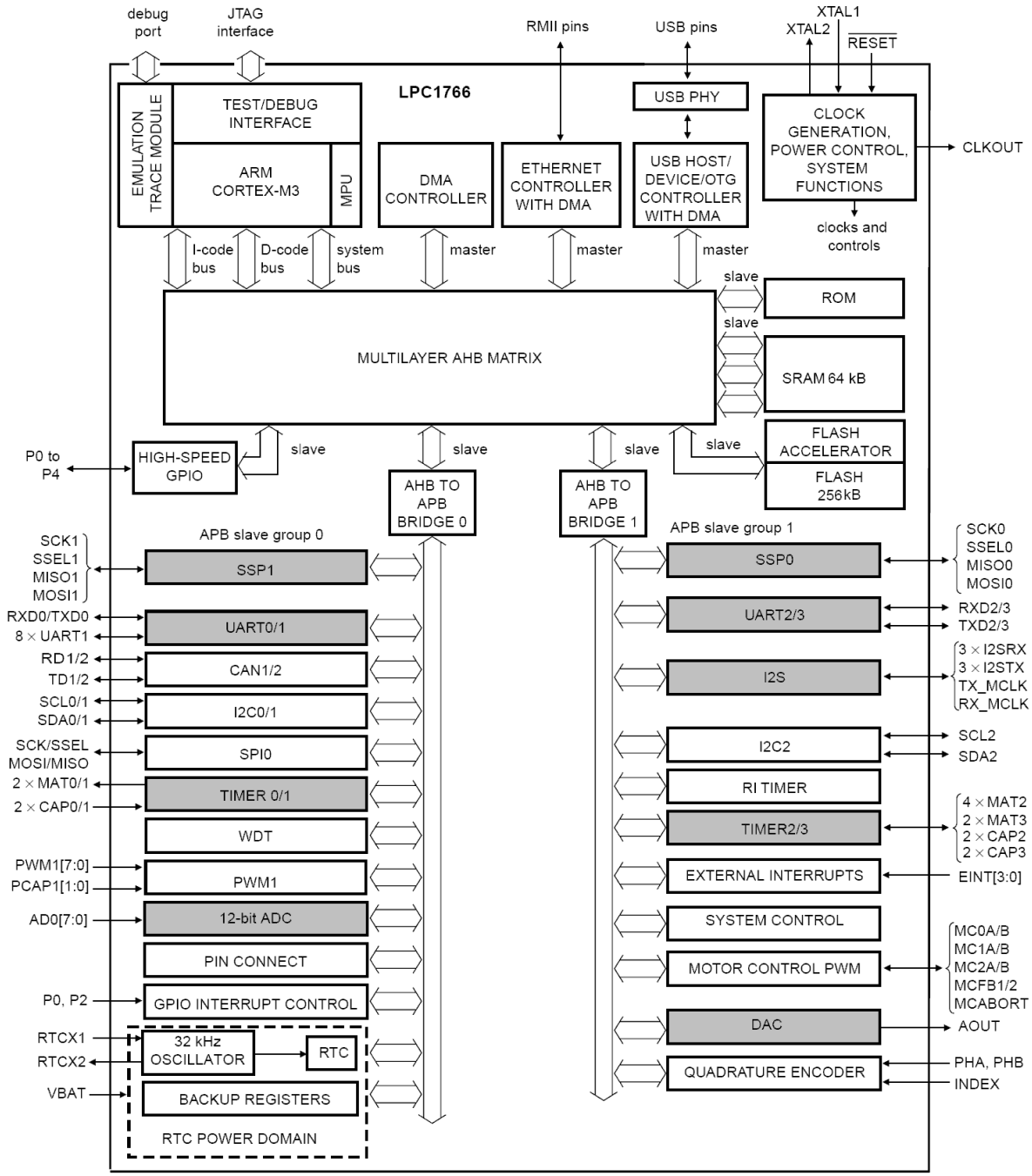
**LPC1766-STK** board use ARM 32-bit Cortex™-M3 microcontroller **LPC1766FBD100** from NXP Semiconductors with these features:

- ARM Cortex-M3 processor, running at frequencies of up to 100 MHz. A Memory Protection Unit (MPU) supporting eight regions is included.
- ARM Cortex-M3 built-in Nested Vectored Interrupt Controller (NVIC).
- 256 kB on-chip flash programming memory. Enhanced flash memory accelerator enables high-speed 100 MHz operation with zero wait states.
- In-System Programming (ISP) and In-Application Programming (IAP) via on-chip bootloader software.
- On-chip SRAM includes:
    - 32 kB of SRAM on the CPU with local code/data bus for high-performance CPU access.
    - Two 16 kB SRAM blocks with separate access paths for higher throughput. These SRAM blocks may be used for Ethernet, USB, and DMA memory, as well as for general purpose CPU instruction and data storage.
- Eight channel General Purpose DMA controller (GPDMA) on the AHB multilayer matrix that can be used with the SSP, I2S-bus, UART, the Analog-to-Digital and Digital-to-Analog converter peripherals, timer match signals, and for memory-to-memory transfers.
- Multilayer AHB matrix interconnect provides a separate bus for each AHB master. AHB masters include the CPU, General Purpose DMA controller, Ethernet MAC, and the USB nterface. This interconnect provides communication with no arbitration delays.

- Split APB bus allows high throughput with few stalls between the CPU and DMA.
- Serial interfaces:
  - Ethernet MAC with RMII interface and dedicated DMA controller.
  - USB 2.0 full-speed device/Host/OTG controller with dedicated DMA controller and on-chip PHY for device, Host, and OTG functions.
  - Four UARTs with fractional baud rate generation, internal FIFO, DMA support, and RS-485 support. One UART has modem control I/O, and one UART has IrDA support.
  - CAN 2.0B controller with two channels.
  - SPI controller with synchronous, serial, full duplex communication and programmable data length.
  - Two SSP controllers with FIFO and multi-protocol capabilities. The SSP interfaces can be used with the GPDMA controller.
  - Two I2C-bus interfaces supporting fast mode with a data rate of 400 kbits/s with multiple address recognition and monitor mode.
  - One I2C-bus interface supporting full I2C-bus specification and fast mode plus with a data rate of 1 Mbit/s with multiple address recognition and monitor mode.
  - I2S (Inter-IC Sound) interface for digital audio input or output, with fractional rate control. The I2S-bus interface can be used with the GPDMA. The I2S-bus interface supports 3-wire and 4-wire data transmit and receive as well as master clock input/output.
- Other peripherals:
  - 70 General Purpose I/O (GPIO) pins with configurable pull-up/down resistors and a new, configurable open-drain operating mode.
  - 12-bit Analog-to-Digital Converter (ADC) with input multiplexing among eight pins, conversion rates up to 1 MHz, and multiple result registers. The 12-bit ADC can be used with the GPDMA controller.
  - 10-bit Digital-to-Analog Converter (DAC) with dedicated conversion timer and DMA support.
  - Four general purpose timers/counters, with a total of eight capture inputs and ten compare outputs. Each timer block has an external count input and DMA support.
  - One motor control PWM with support for three-phase motor control.
  - Quadrature encoder interface that can monitor one external quadrature encoder.
  - One standard PWM/timer block with external count input.
  - RTC with a separate power domain and dedicated RTC oscillator. The RTC block includes 64 bytes of battery-powered backup registers.
  - Watchdog Timer (WDT) resets the microcontroller within a reasonable amount of time if it enters an erroneous state.
  - System tick timer, including an external clock input option.

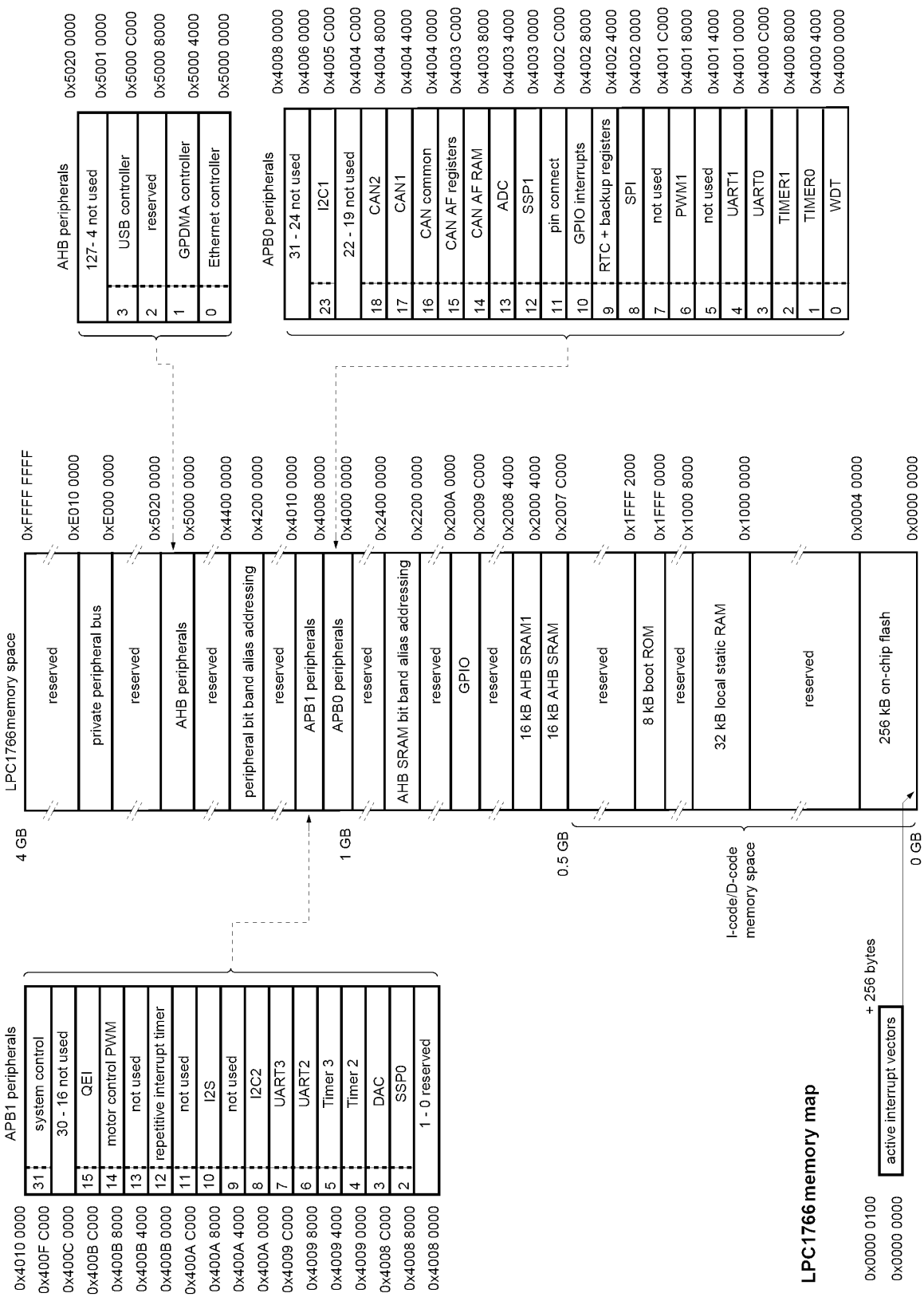
    - Repetitive interrupt timer provides programmable and repeating timed interrupts.
    - Each peripheral has its own clock divider for further power savings.
- Standard JTAG test/debug interface for compatibility with existing tools. Serial Wire Debug and Serial Wire Trace Port options.
- Emulation trace module enables non-intrusive, high-speed real-time tracing of instruction execution.
- Integrated PMU (Power Management Unit) automatically adjusts internal regulators to minimize power consumption during Sleep, Deep sleep, Power-down, and Deep power-down modes.
- Four reduced power modes: Sleep, Deep-sleep, Power-down, and Deep power-down.
- Single 3.3 V power supply (2.4 V to 3.6 V).
- Four external interrupt inputs configurable as edge/level sensitive. All pins on PORT0 and PORT2 can be used as edge sensitive interrupt sources.
- Non-maskable Interrupt (NMI) input.
- Clock output function that can reflect the main oscillator clock, IRC clock, RTC clock, CPU clock, and the USB clock.
- The Wakeup Interrupt Controller (WIC) allows the CPU to automatically wake up from any priority interrupt that can occur while the clocks are stopped in deep sleep, Power-down, and Deep power-down modes.
- Processor wake-up from Power-down mode via interrupts from various peripherals.
- Brownout detect with separate threshold for interrupt and forced reset.
- Power-On Reset (POR).
- Crystal oscillator with an operating range of 1 MHz to 25 MHz.
- 4 MHz internal RC oscillator trimmed to 1 % accuracy that can optionally be used as a system clock.
- PLL allows CPU operation up to the maximum CPU rate without the need for a high-frequency crystal. May be run from the main oscillator, the internal RC oscillator, or the RTC oscillator.
- USB PLL for added flexibility.
- Code Read Protection (CRP) with different security levels.

# BLOCK DIAGRAM:

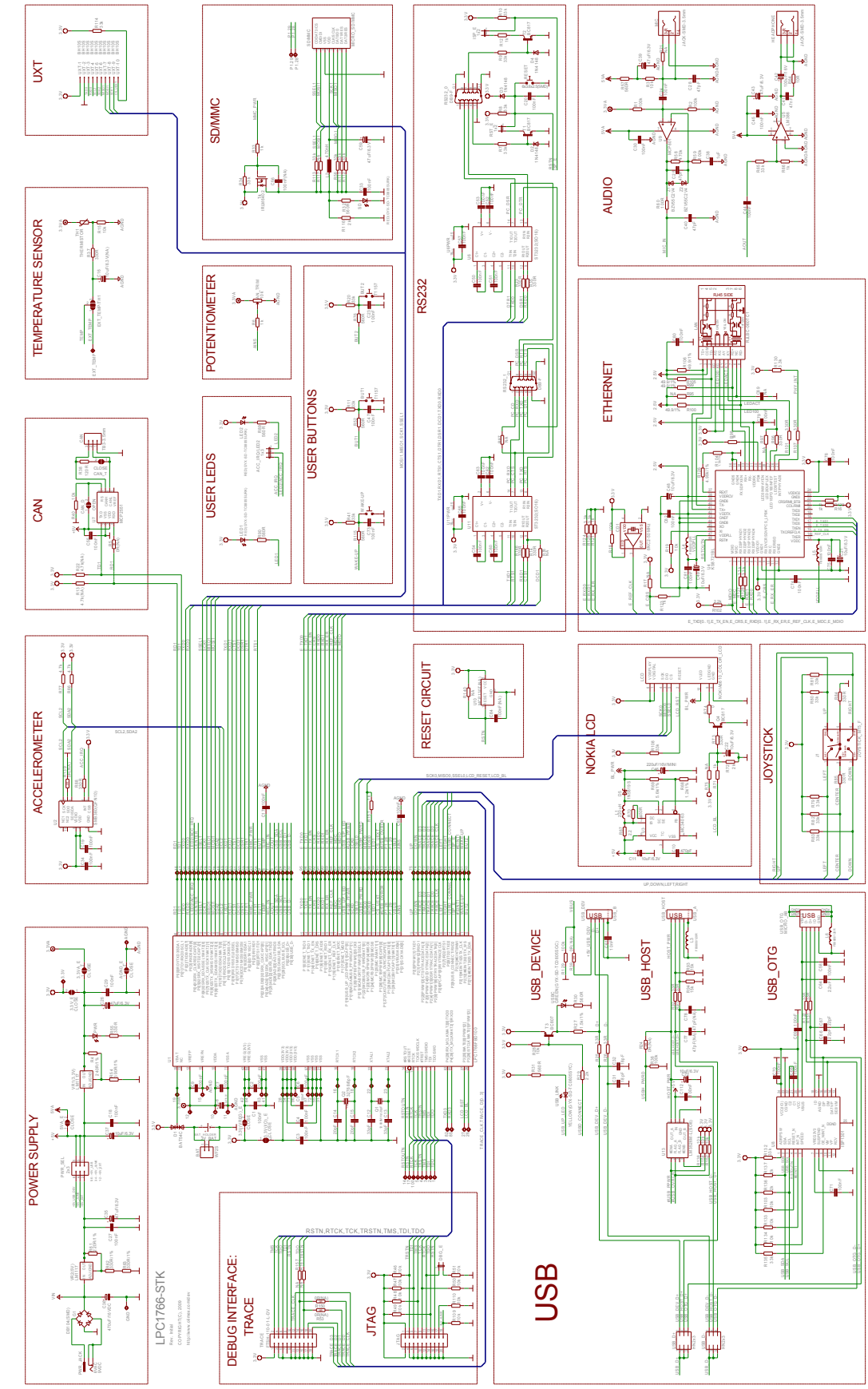



Grey-shaded blocks represent peripherals with connection to the GPDMA.

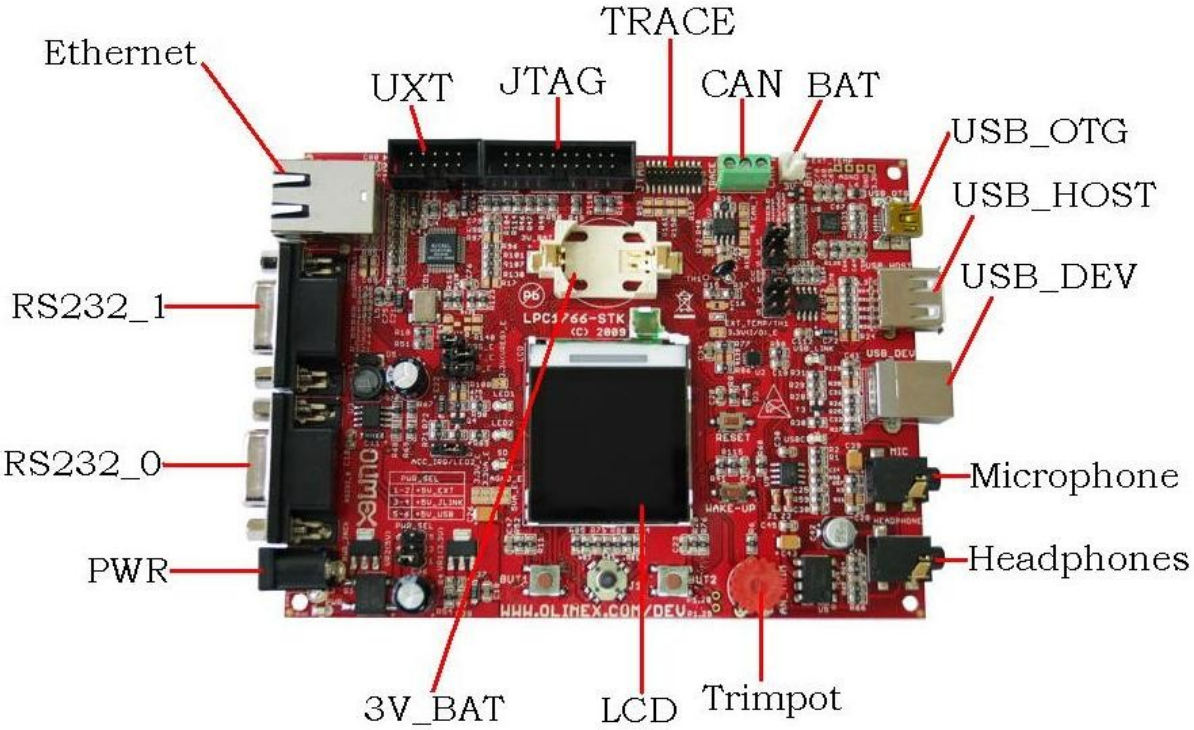
# MEMORY MAP:

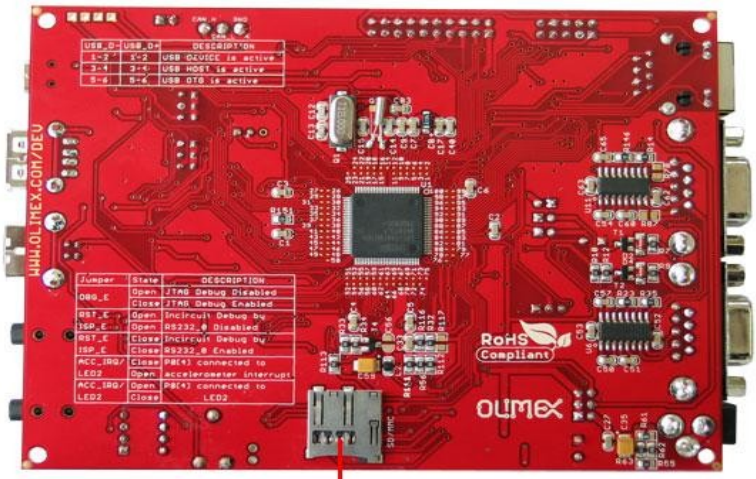

LPC1766 memory space
4 GB
1 GB
0.5 GB
0 GB
0xFFFF FFFF
0xE010 0000
0xE000 0000
0x5020 0000
0x5000 0000
0x4400 0000
0x4200 0000
0x4010 0000
0x4008 0000
0x4000 0000
0x2400 0000
0x2200 0000
0x200A 0000
0x2009 C000
0x2008 4000
0x2000 4000
0x2007 C000
0x1FFF 2000
0x1FFF 0000
0x1000 8000
0x1000 0000
0x0004 0000
0x0000 0000
reserved
private peripheral bus
reserved
AHB peripherals
reserved
peripheral bit band alias addressing
reserved
APB1 peripherals
APB0 peripherals
reserved
AHB SRAM bit band alias addressing
reserved
GPIO
reserved
16 kB AHB SRAM1
16 kB AHB SRAM
reserved
8 kB boot ROM
reserved
32 kB local static RAM
reserved
256 kB on-chip flash
I-code/D-code memory space
AHB peripherals
0x5020 0000
0x5001 0000
0x5000 C000
0x5000 8000
0x5000 4000
0x5000 0000
127- 4 not used
3 USB controller
2 reserved
1 GPDMA controller
0 Ethernet controller
APB0 peripherals
0x4008 0000
0x4006 0000
0x4005 C000
0x4004 C000
0x4004 8000
0x4004 4000
0x4004 0000
0x4003 C000
0x4003 8000
0x4003 4000
0x4003 0000
0x4002 C000
0x4002 8000
0x4002 4000
0x4002 0000
0x4001 C000
0x4001 8000
0x4001 4000
0x4001 0000
0x4000 C000
0x4000 8000
0x4000 4000
0x4000 0000
31 - 24 not used
23 I2C1
22 - 19 not used
18 CAN2
17 CAN1
16 CAN common
15 CAN AF registers
14 CAN AF RAM
13 ADC
12 SSP1
11 pin connect
10 GPIO interrupts
9 RTC + backup registers
8 SPI
7 not used
6 PWM1
5 not used
4 UART1
3 UART0
2 TIMER1
1 TIMER0
0 WDT
APB1 peripherals
0x4010 0000
0x400F C000
0x400C 0000
0x400B C000
0x400B 8000
0x400B 4000
0x400B 0000
0x400A C000
0x400A 8000
0x400A 4000
0x400A 0000
0x4009 C000
0x4009 8000
0x4009 4000
0x4009 0000
0x4008 C000
0x4008 8000
0x4008 0000
31 system control
30 - 16 not used
15 QEI
14 motor control PWM
13 not used
12 repetitive interrupt timer
11 not used
10 I2S
9 not used
8 I2C2
7 UART3
6 UART2
5 Timer 3
4 Timer 2
3 DAC
2 SSP0
1 - 0 reserved
LPC1766 memory map
0x0000 0100
0x0000 0000
active interrupt vectors
+ 256 bytes

# SCHEMATIC:


UXT
SD/MMC
RS232
AUDIO
TEMPERATURE SENSOR
POTENTIOMETER
ETHERNET
USER LEDS
USER BUTTONS
CAN
RESET CIRCUIT
NOKIA LCD
JOYSTICK
ACCELEROMETER
POWER SUPPLY
LPC1766-STK
DEBUG INTERFACE:
TRACE
JTAG
USB
USB_DEVICE
USB_HOST
USB_OTG

## BOARD LAYOUT:




## POWER SUPPLY CIRCUIT:

**LPC1766-STK** is typically power supplied with 9 VDC.

The programmed board power consumption is about 200 mA with all peripherials enabled

## RESET CIRCUIT:

**LPC1766-STK** reset circuit includes jumper RST_E, pin 15 of JTAG connector, pin 10 of TRACE connector and RESET button.

## CLOCK CIRCUIT:

Quartz crystal 12 MHz is connected to LPC1766 pin 22 (XTAL1) and pin 23 (XTAL2).

Quartz crystal 32.768 kHz is connected to LPC1766 pin 16 (RTCX1) and pin 18 (RTCX2).

## JUMPER DESCRIPTION:

### CAN_D

CAN Disable. If this jumper is closed, the CAN is disabled.
Default state is open.

### CAN_T

This jumper assures correct work of the CAN. At each end of the bus it should be closed. This means that if you have only two devices with CAN, the jumpers of both devices should be closed. If you have more than two devices, only the two end-devices should be closed.
Default state is closed.

### 3.3V(VREG)_E

This jumper, when closed, supplies 3.3 V voltage for the on-chip voltage regulator only – 42 and 84 pins of the MCU.
Default state is closed.

### 3.3V_E

This jumper, when closed, enable the main 3.3 V regulator VR1(3.3V) - LM1117.
Default state is closed.

### 3.3VA_E

This jumper, when closed, supplies 3.3 V voltage to the VDDA and VREFP pins of the MCU.
Default state is closed.

### 3.3V(I/O)_E

This jumper, when closed, supplies 3.3 V voltage to the VDD – 4 pins of the MCU.
Default state is closed.

## 5VA_E


This jumper, when closed, supplies analog 5V voltage supply to the audio amplifiers.
Default state is closed.

## AGND_E


This jumper, when closed, connects analog GND to the GND of the MCU.
Default state is closed.

## EXT_TEMP/TH1


This jumper, when is in position EXT_TEMP – takes signal from external temperature sensor and when is in position TH1 – takes signal from the thermistor TH1 of the board.

Default state is in position TH1.

## DBG_E


The position of this jumper doesn't matter.
Default state is closed.

## RST_E


This jumper, when closed, enables programing via RS232.
Default state is open.

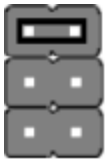
## ISP_E


This jumper, when closed, enables programing via RS232.
Default state is open.

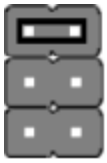
## ACC_IRQ/LED2


This jumper when is in position ACC_IRQ – enables interrupt request from the accelerometer and when is in position LED2 – enables LED2.
Default state is LED2.

## USB_D-

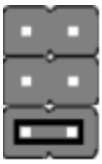

This jumper, when1-2 are shorted – enables USB DEVICE, when 3-4 are shorted– enables USB HOST and when 5-6 are shorted – enables USB OTG.
Default state is 1-2.

## USB_D+



This jumper, when1-2 are shorted – enables USB DEVICE, when 3-4 are shorted– enables USB HOST and when 5-6 are shorted – enables USB OTG.
Default state is 1-2.

## PWR_SEL



When 1-2 are shorted – the board is supplied from PWR_JACK, when 3-4 are shorted – the board is supplied from JTAG and when 5-6 are shorted – the board is supplied from USB_DEV.
Default state is 1-2.

# INPUT/OUTPUT:

**LED1 (red)** connected to LPC1766 pin 39 (P1[25]/MC1A/MAT1[1]).

**LED2 (red)** connected to LPC1766 pin 81 (P0[4]/I2SRX_CLK/RD2/CAP2[0]) via jumper ACC_IRQ/LED2, when this jumper is in position LED2.

**SD/MMC LED (red)** connected to **SD/MMC** pin 4 (VDD).

**Power-on LED (red)** with name **PWR** – this LED shows that +3.3V is applied to the board.

**USB_UP_LED** with name **USB_LINK (yellow)** connected to **LPC1766** pin 32 (P1[18]/USB_UP_LED/PWM1[1]/CAP1[0]).

**USBD_CONNECT LED** with name **USBC(green)** connected to **LPC1766** pin 64 (P2[9]/USB_CONNECT/RXD2) through T3 and R29.

**User button** with name **BUT1** connected to **LPC1766** pin 9 (P0[23]/AD0[0]/I2SRX_CLK/CAP3[0]).

**User button** with name **BUT2** connected to **LPC1766** pin 50 (P2[13]/#EINT3/I2STX_SDA).

**User button** with name **WAKE-UP** connected to **LPC1766** pin 51 (P2[12]/#EINT2/I2STX_WS).

**User button** with name **RESET** connected to **LPC1766** pin 17 (#RESET).

**Joystick button** with name **J1** this is 4 directions plus center button, in the schematic the joystick four directions switches are connected through 33k resistors to **LPC1766** pins - 65 (P2[8]/TD2/TXD2) – RIGHT, 66 (P2[7]/RD2/RTS1) – LEFT, 74 (P2[1]/PWM1[2]/RXD1) – DOWN, 75 (P2[0]/PWM1[1]/TXD1) – UP, the center button is connected to pin 80 (P0[5]/I2SRX_WS/TD2/CAP2[1]).

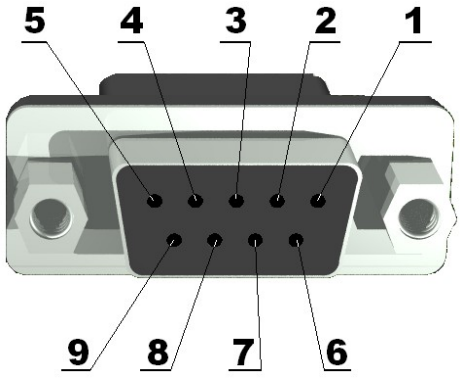
**Trimpot** with name **AN_TRIM** connected to **LPC1766** pin 20 (P1[31]/SCK1/AD0[5]).

**TFT LCD -** 128x128 12 bit color with backlight.

## EXTERNAL CONNECTORS DESCRIPTION:

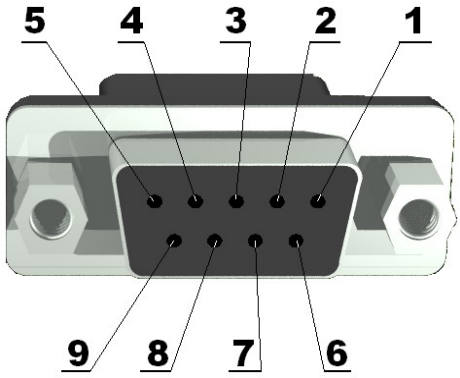
### RS232_0:

| Pin # | Signal Name |
|---|---|
| 1 | NC |
| 2 | T2OUT |
| 3 | R2IN |
| 4 | RST_E |
| 5 | GND |
| 6 | NC |
| 7 | ISP_E |
| 8 | NC |
| 9 | NC |



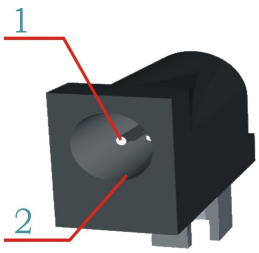

### RS232_1:

| Pin # | Signal Name |
|---|---|
| 1 | PC_CD |
| 2 | PC_RXD |
| 3 | PC_TXD |
| 4 | PC_DTR |
| 5 | GND |
| 6 | PC_DSR |
| 7 | PC_RTS |
| 8 | PC_CTS |
| 9 | NC |



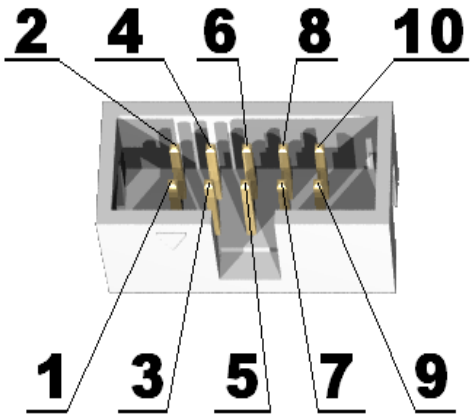
## PWR_JACK:

| Pin # | Signal Name |
|---|---|
| 1 | Power Input |
| 2 | GND |




## UXT:

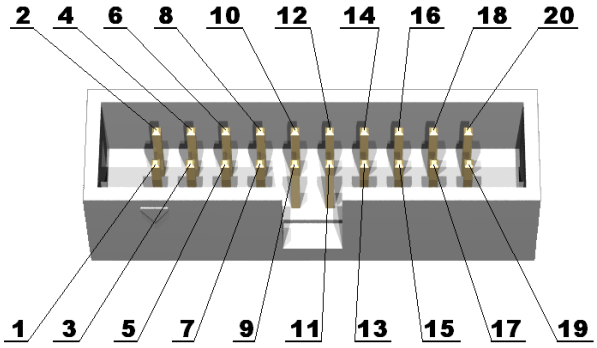
| Pin # | Signal Name |
|---|---|
| 1 | 3.3V |
| 2 | GND |
| 3 | TXD3 |
| 4 | RXD3 |
| 5 | SCL2 |
| 6 | SDA2 |
| 7 | MISO1 |
| 8 | MOSI1 |
| 9 | SCK1 |
| 10 | CS_UEXT |




## JTAG:

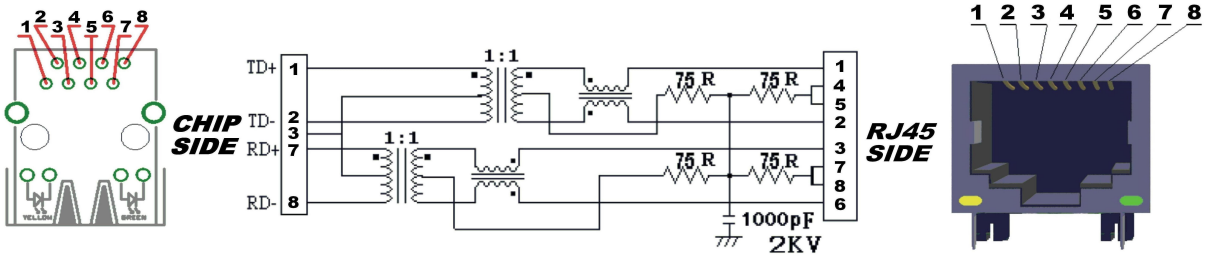
The JTAG connector allows the software debugger to talk via a JTAG (Joint Test Action Group) port directly to the core. Instructions may be inserted and executed by the core thus allowing LPC1766 memory to be programmed with code and executed step by step by the host software.

For more details refer to IEEE Standard 1149.1 - 1990 Standard Test Access Port and Boundary Scan Architecture and LPC1766 datasheets and users manual.




| Pin # | Signal Name | Pin # | Signal Name |
|---|---|---|---|
| 1 | 3.3V | 2 | 3.3V |
| 3 | TRSTN | 4 | GND |
| 5 | TDI | 6 | GND |
| 7 | TMS | 8 | GND |
| 9 | TCK | 10 | GND |
| 11 | RTCK | 12 | GND |
| 13 | TDO | 14 | GND |
| 15 | RSTN | 16 | GND |
| 17 | through 10K to GND | 18 | GND |
| 19 | +5V_JLINK | 20 | GND |

## LAN:



| Pin # | Signal Name Chip Side | Pin # | Signal Name Chip Side |
|---|---|---|---|
| 1 | TPOUT+ | 5 | Not Connected (NC) |
| 2 | TPOUT- | 6 | Not Connected (NC) |
| 3 | 2.5V | 7 | TPIN+ |
| 4 | Not Connected (NC) | 8 | TPIN- |

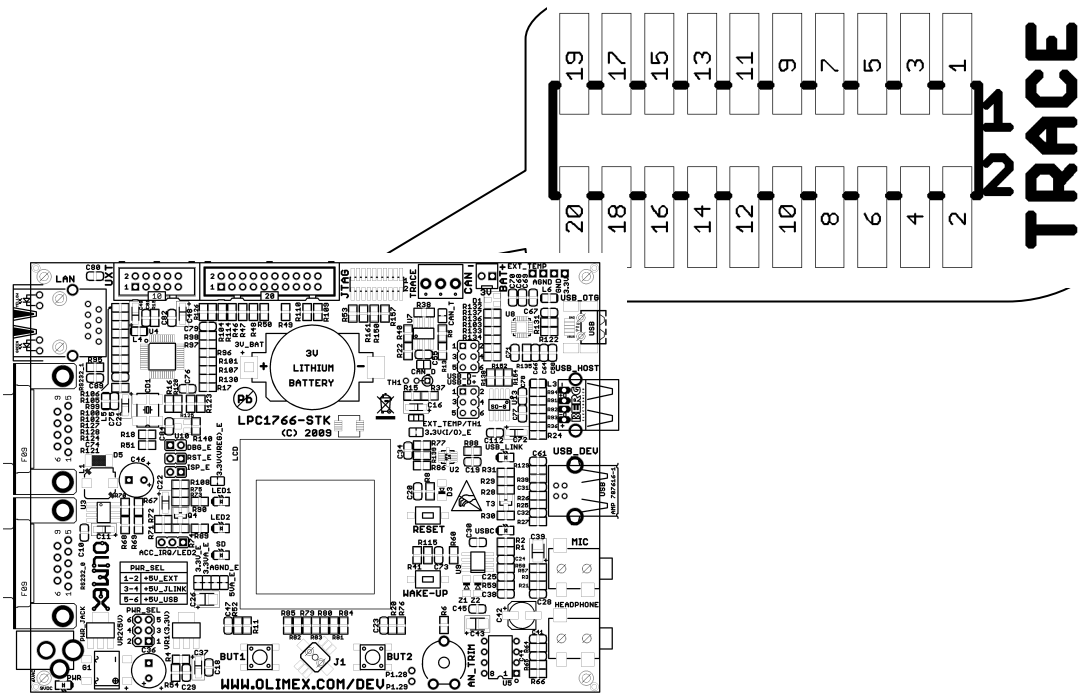
| LED | Color | Usage |
|---|---|---|
| Right | Yellow | Activity |
| Left | Green | 100MBits/s (Half/Full duplex) |

## CAN

| Pin# | Signal | Description |
|---|---|---|
| 1 | GND | Ground |
| 2 | CANL | CAN LOW |
| 3 | CANH | CAN HIGH |

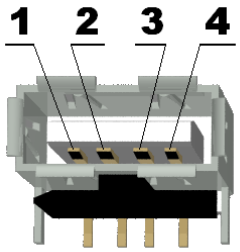

## TRACE

| Pin# | Signal | Description | Pin# | Signal | Description |
|---|---|---|---|---|---|
| 1 | VCC | 3,3V | 2 | TMS | |
| 3 | GND | | 4 | TCK | |
| 5 | GND | | 6 | TDO | |
| 7 | NC | | 8 | TDI | |
| 9 | GND | | 10 | RSTN | |
| 11 | GND | | 12 | TRACE_CLK | |
| 13 | GND | | 14 | TRACE_D0/TDO | Depends on R150/R157 |
| 15 | GND | | 16 | TRACE_D1/TRST | Depends on R153/R161 |
| 17 | GND | | 18 | TRACE_D2 | |
| 19 | GND | | 20 | TRACE_D3 | |


19
17
15
13
11
9
7
5
3
1
20
18
16
14
12
10
8
6
4
2
TRACE
LAN
JTAG
TRACE
CAN
USB_OTG
USB_HOST
USB_DEV
USB_LINK
3V
LITHIUM
BATTERY
LPC1766-STK
(C) 2009
RESET
WAKE-UP
MIC
HEADPHONE
BUT1
BUT2
J1
WWW.OLIMEX.COM/DEV

## USB_HOST

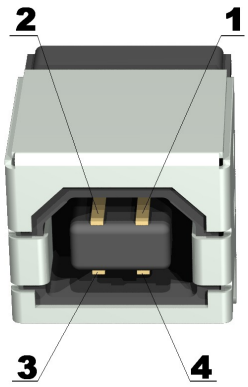
| Pin # | Signal Name |
|---|---|
| 1 | HOST_PWR |
| 2 | USB_HOST_D- |
| 3 | USB_HOST_D+ |
| 4 | GND |




USB 2.0 full-speed Host controller with dedicated DMA controller and on-chip PHY. The host controller enables full- and low-speed data exchange with USB devices attached to the bus. It consists of a register interface, a serial interface engine, and a DMA controller. The register interface complies with the OHCI specification.

## USB_DEVICE

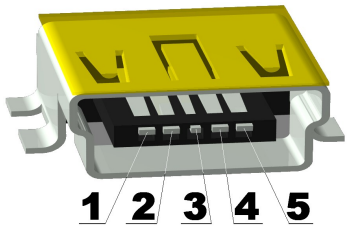
| Pin # | Signal Name |
|---|---|
| 1 | +5V_USB_DEV |
| 2 | USB_DEV_D- |
| 3 | USB_DEV_D+ |
| 4 | GND |




The device controller enables 12 Mbit/s data exchange with a USB Host controller. It consists of a register interface, serial interface engine, endpoint buffer memory, and a DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate endpoint buffer. The status of a completed USB transfer or error condition is indicated via status registers. An interrupt is also generated if enabled. When enabled, the DMA controller transfers data between the endpoint buffer and the on-chip SRAM.

## USB_OTG

| Pin # | Signal Name |
|---|---|
| 1 | VBUS |
| 2 | USB_OTG_D- |
| 3 | USB_OTG_D+ |
| 4 | USB_OTG_ID |
| 5 | GND |

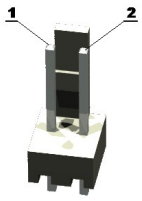



USB OTG is a supplement to the USB 2.0 specification that augments the capability of existing mobile devices and USB peripherals by adding host functionality for connection to USB peripherals.

The OTG Controller integrates the host controller, device controller, and a master-only I2C-bus interface to implement OTG dual-role device functionality. The dedicated I2C-bus interface controls an external OTG transceiver.

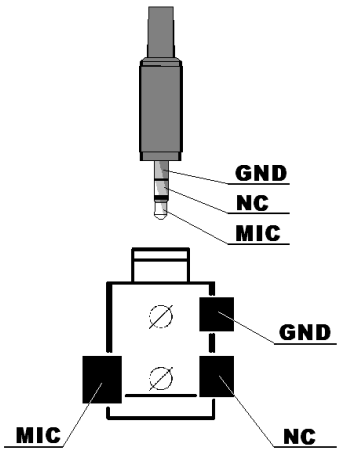
## BAT

| Pin # | Signal Name |
|---|---|
| 1 | to 3.3V |
| 2 | GND |



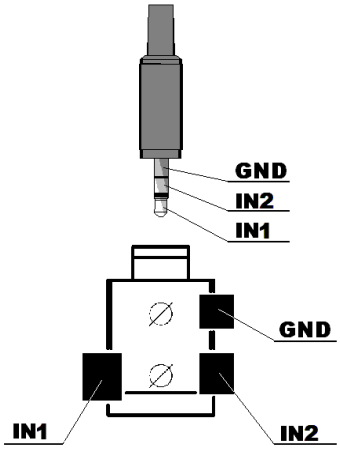

## MIC

| Pin # | Signal Name |
|---|---|
| 1 | AGND |
| 2 | NC |
| 3 | MIC |



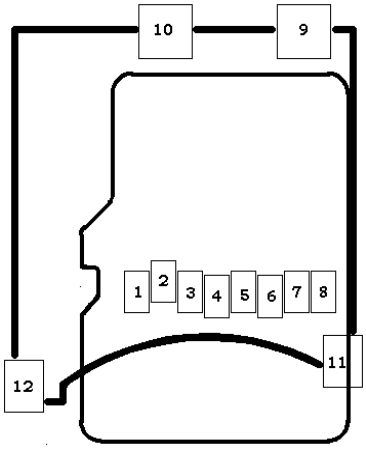
## HEADPHONE

| Pin # | Signal Name |
|---|---|
| 1 | AGND |
| 2 | IN1=IN2 |
| 3 | IN2=IN1 |

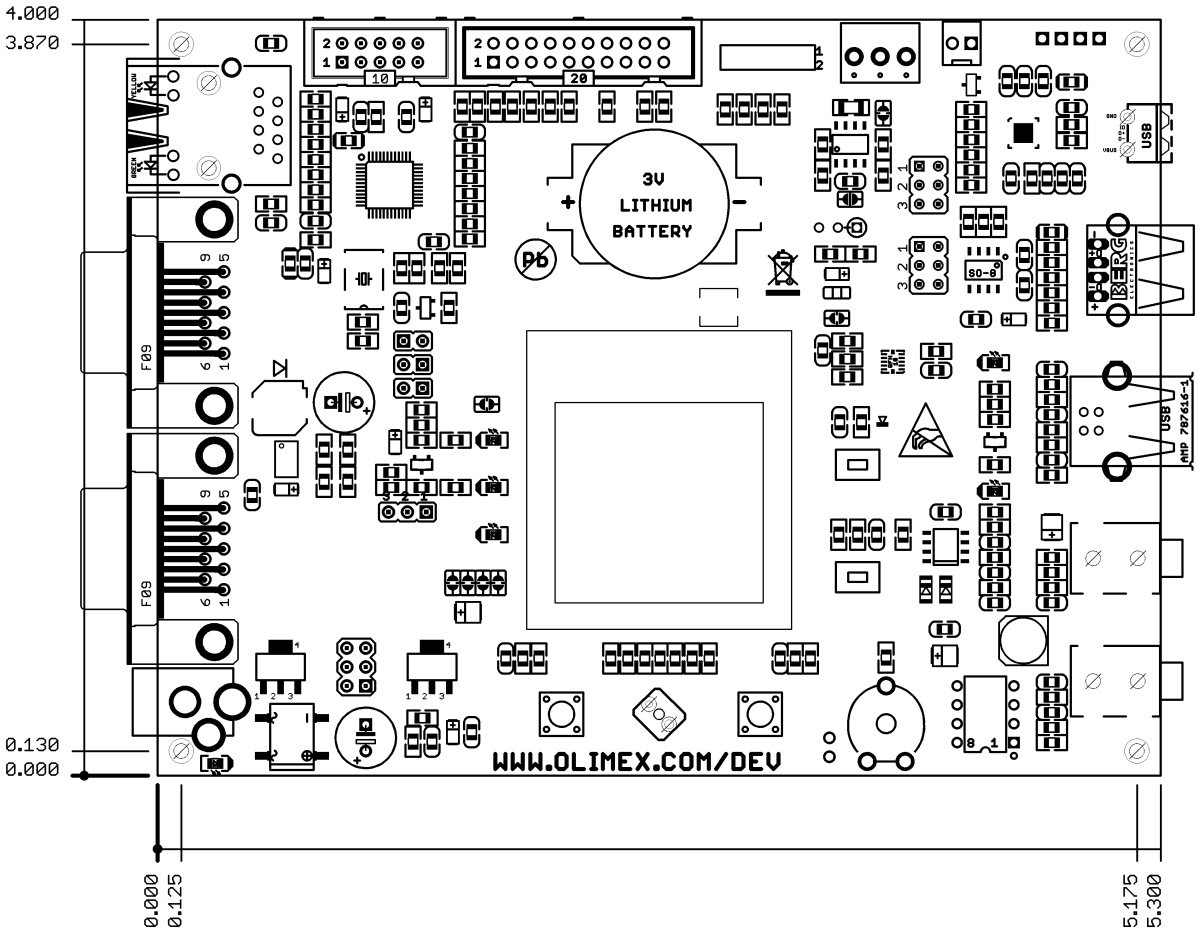



## SD/MMC

| Pin # | Signal Name |
|---|---|
| 1 | Pull-up |
| 2 | SSEL1 |
| 3 | MOSI1 |
| 4 | VDD (power supply) |
| 5 | SCK1 |
| 6 | GND |
| 7 | MISO1 |
| 8 | Pull-up |
| 9 | Not connected |
| 10 | Not connected |
| 11 | Not connected |
| 12 | Not connected |



# MECHANICAL DIMENSIONS:




All measures are in Inches.

## AVAILABLE DEMO SOFTWARE:

- **Accelerometer Demo** - Basic use of I/O, timer, interrupt controllers, LDC module and the on board accelerometer EW-ARM 5.40.
- **Audio Device Class** - USB audio device class with one output and one input EW-ARM 5.40.
- **Getting Started** - Basic use of I/O, timer and interrupt controllers EW-ARM 5.40.
- **LCD Demo** - Basic use of the I/O, timer, interrupt controllers and LDC module for graphic and text drawing EW-ARM 5.40.
- **Mass Storage Class** - USB mass storage class with MMC/SD card drive EW-ARM 5.40.
- **Simple periherals** - Simple ADC demo, Basic use of ADC, Simple DAC demo, Basic use of DAC, Simple DMA demo, Basic use of DMA, Simple EMAC demo, Basic use of EMAC, Simple EXTINT demo, Basic use of EXTINT, Simple GPIO demo, Basic use of GPIO, Simple RTC demo, Basic use of RTC, Simple SSP demo, Basic use of SSP, Simple Timer demo, Basic use of Timer, Simple UART demo, Basic use of UART, Simple WDT demo, Basic use of WDT EW-ARM 5.40.
- **uIP WEB Server** - WEB server application running on the top of the uIP 1.0 TCP-IP stack EW-ARM 5.40.
- **USB Host Demo** - USB host masstorage class framework EW-ARM 5.40.
- **USB Mouse** - USB HID class (Mouse) EW-ARM 5.40.
- **Virtual COM Port** - USB communication device class EW-ARM 5.40.

## ORDER CODE: LPC-1766STK - assembled and tested board

**How to order?**

You can order to us directly or by any of our distributors.
Check our web www.olimex.com/dev for more info.

## Revision history:

Revision Initial, October 2009

**Disclaimer:**